What is claimed is:

1. An electronic device comprising:

a substrate; and

a dielectric layer disposed on the substrate, the dielectric layer containing a TiO_x layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation.

2. The electronic device of claim 1, wherein the lanthanide has a concentration in the dielectric layer of between about 10% and about 30% of the dielectric layer.

3. The electronic device of claim 1, wherein the dielectric layer has a dielectric constant ranging from about 50 to about 110.

4. The electronic device of claim 1, wherein the dielectric layer has an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

5. An electronic device comprising:

a substrate; and

a dielectric layer disposed on the substrate, the dielectric layer containing a TiO_x layer doped with Nd, wherein the TiO_x layer is formed by ion assisted electron beam evaporation.

6. The electronic device of claim 5, wherein the dielectric layer has a Nd doping of between about 10% and about 30% of the dielectric layer.

7. The electronic device of claim 5, wherein the TiO_x layer doped with Nd has a dielectric constant ranging from about 50 to about 110.

8. The electronic device of claim 5, wherein the dielectric layer has an equivalent oxide thickness (t_{eq}) of less than 3 Angstroms.

9. An electronic device comprising:

a substrate; and

a dielectric layer disposed on the substrate, the dielectric layer containing a TiO_x layer doped with Tb, wherein the TiO_x layer is formed by ion assisted electron beam evaporation.

10. The electronic device of claim 9, wherein the TiO_x layer has a Tb concentration of between about 10% and about 30% of the TiO_x layer.

11. The electronic device of claim 9, wherein the dielectric layer has a dielectric constant ranging from about 50 to about 110.

12. The electronic device of claim 9, wherein the dielectric layer has an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

13. An electronic device comprising:

a substrate; and

a dielectric layer disposed on the substrate, the dielectric layer containing a TiO_x layer doped with Dy, wherein the TiO_x layer is formed by ion assisted electron beam evaporation.

14. The electronic device of claim 13, wherein the dielectric layer has a Dy concentration of between about 10% and about 30% of the dielectric layer.

15. The electronic device of claim 13, wherein the TiO_x layer has a dielectric constant ranging from about 50 to about 110.

16. The electronic device of claim 13, wherein the dielectric layer has an equivalent oxide thickness (t_{eq}) of less than 20 Angstroms.

17. A transistor comprising:

a source region disposed in a substrate;

a drain region disposed in the substrate;

a body region located between the source region and the drain region;

a dielectric layer disposed on the body region between the source region and the drain region, the dielectric layer containing a TiO_x layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation; and

a gate coupled to the dielectric layer.

18. The transistor of claim 17, wherein the dielectric layer containing the TiO_x layer doped with the lanthanide includes a TiO_x layer doped with one or more of Nd, Tb, and Dy.

19. The transistor of claim 17, wherein the dielectric layer is substantially amorphous.

20. The transistor of claim 17, wherein the dielectric layer exhibits a dielectric constant in the range from about 50 to about 110.

21. The transistor of claim 17, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms.

22. The transistor of claim 17, wherein the dielectric layer exhibits an equivalent oxide thickness (t_{eq}) of less than 3 Angstroms.

23. The transistor of claim 17, wherein the transistor further includes:

a floating gate situated between the body region and the gate; and

a floating gate dielectric disposed on the floating gate with the gate disposed on the floating gate dielectric, the floating gate dielectric having a TiO_x layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation.

24. The transistor of claim 17, wherein the transistor is a floating gate transistor.

25. A capacitor comprising:

a first conductive layer disposed on a substrate;

a dielectric layer disposed on the first conductive layer, the dielectric layer containing a TiOx layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation; and

a second conductive layer disposed on the dielectric layer.

26. The capacitor of claim 25, wherein the dielectric layer containing the TiO_x layer doped with the lanthanide includes a TiO_x layer doped with one or more of Nd, Tb, and Dy.

27. The capacitor of claim 25, wherein the dielectric layer is substantially amorphous.

28. The capacitor of claim 25, wherein the dielectric layer exhibits a dielectric constant in the range from about 50 to about 110.

29. A memory comprising:

a number of access transistors, each access transistor having a source region disposed in a substrate, a drain region disposed in the substrate, and a gate, at least one access transistor including a dielectric layer disposed on the substrate with the gate disposed on the dielectric layer, the dielectric layer containing a TiOx layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the source regions of the number of access transistors; and

a number of bit lines coupled to a number of the drain regions of the number of access transistors.

30. The memory of claim 29, wherein the dielectric layer containing the TiO_x layer doped with the lanthanide includes a TiO_x layer doped with one or more of Nd, Tb, and Dy.

31. The memory of claim 29, wherein the dielectric layer is substantially amorphous.

32. The memory of claim 28, wherein the dielectric layer exhibits a dielectric constant in the range from about 50 to about 110.

33. The memory of claim 28, wherein the memory is a dynamic random access memory.

34. The memory of claim 28, wherein the memory is a flash memory.

35. An electronic system, comprising:

a processor;

a system bus; and

a memory array coupled to the processor by the system bus, the memory array including:

a number of access transistors, each access transistor having a source region disposed in a substrate, a drain region disposed in the substrate, and a gate, at least one access transistor including a dielectric layer disposed on the substrate with the gate disposed on the dielectric layer, the dielectric layer containing a TiOx layer doped with a lanthanide, wherein the TiO_x layer is formed by ion assisted electron beam evaporation;

a number of word lines coupled to a number of the gates of the number of access transistors;

a number of source lines coupled to a number of the source regions of the number of access transistors; and

a number of bit lines coupled to a number of the drain regions of the number of access transistors.

36. The electronic system of claim 35, wherein the dielectric layer containing the TiO_x layer doped with the lanthanide includes a TiO_x layer doped with one or more of Nd, Tb, and Dy.

37. The electronic system of claim 35, wherein the dielectric layer is substantially amorphous having a dielectric constant in the range from about 50 to about 110.

38. The electronic system of claim 35, wherein the processor is a microprocessor.

39. The electronic system of claim 35, wherein the electronic system is an information handling system.

40. The electronic system of claim 35, wherein the electronic system is a computer.